Au2001: Non-Magnetic Water Meter Sensor

General Description

Au2001 is an inductive sensing IC targeted for water metering applications. It covers a range of working distance required in water meters. The IC supports SPI for simple interface with micro controllers. The IC works on a wide range of supply from 2.8 V-3.6 V. The IC supports two modes – low sensitivity mode for lesser sensing distance and high sensitivity mode for larger sensing distance. The average current is less than 2 uA in low sensitivity mode and less than 5 uA in high sensitivity mode, when triggered once in 70 ms.

The IC is available in 3 mm x 3 mm 16 pin QFN package.

Features

- **Ultra-low power consumption**
- **Operation Temperature Range of -20 °C to 70 °C**
- **3 mm × 3 mm, 16-Pin QFN package**

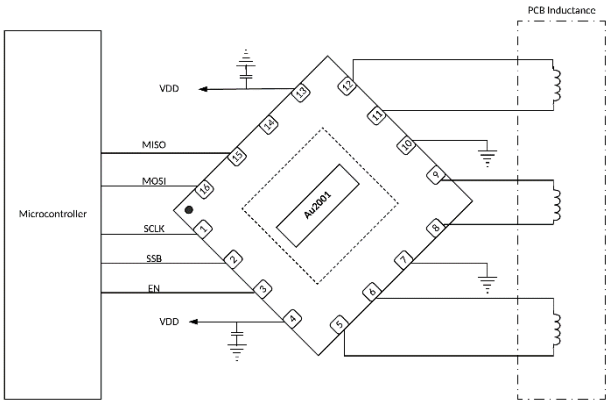

Figure 1 Application Schematic

Applications

- Water Flow Metering

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1 Revision History

Table 1 Revision History

Version	Date	Particulars	Author
0.1	1st October 2019	Document Created	Aura Semi

2 Electrical Specifications

Table 2 Absolute Maximum Ratings

Parameters	Sym	Condition	Min	Typ	Max	Units
Line Supply Voltage		VLINE	-0.3		3.9	V

Table 3 Recommended Operating Conditions

Parameters	Sym	Condition	Min	Typ	Max	Units
Line Supply Voltage		VDD	2.8		3.6	V
Temperature		Operation temperature	-20		70	°C

Table 4 ESD Ratings

Parameter	Sym	Conditions	Min	Typ	Max	Units
Human Body Model	HBM			4000		V
Charged Device Model	CDM			500		V
Latchup	LU			200		mA

3 Pin Configurations / IC Specifications

3.1 Pin Diagram

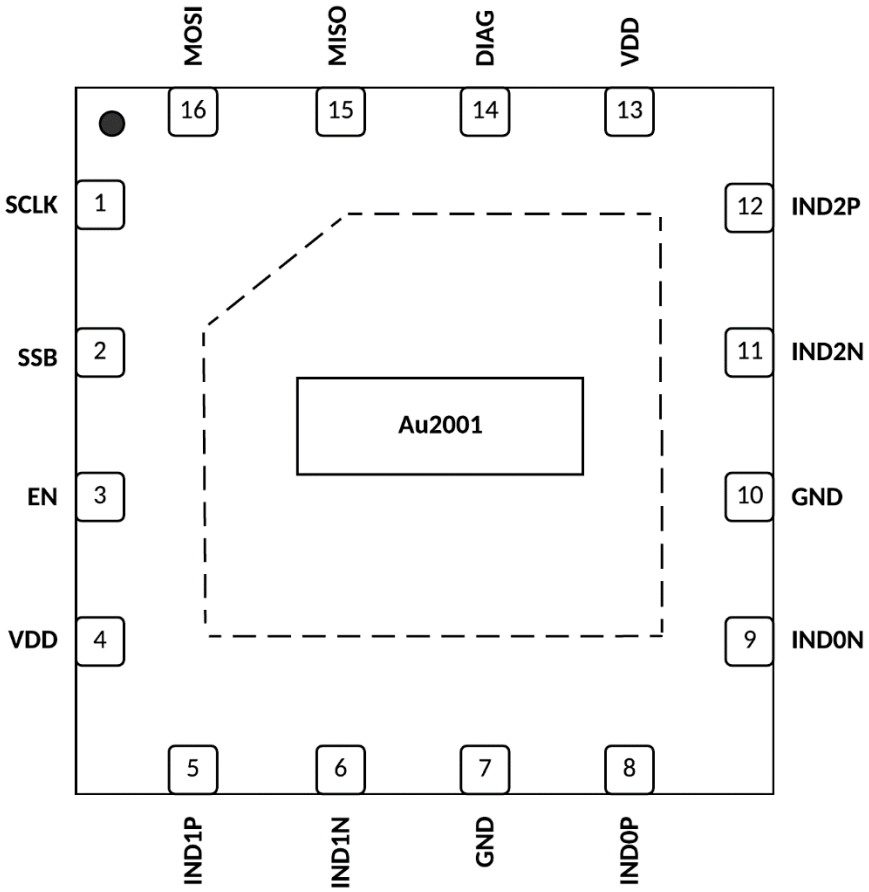

Figure 2 Pin Diagram

3.2 Functional Description

Au2001 is a relative inductance change measurement IC. This is specifically targeted for non-magnetic water flow meters.

3.3 IP PIN Description

Table 5 Pin Functions

Name	No.	Description
IND1P	5	P-terminal of PCB inductance 1
IND1N	6	N-terminal of PCB inductance 1
IND2P	12	P-terminal of PCB inductance 2
IND2N	11	N-terminal of PCB inductance 2
IND0P	8	P-terminal of PCB inductance 0
IND0N	9	N-terminal of PCB inductance 0
VDD	4,13	Supply

GND	7,10	Ground
EN	3	Enable the Sensor
SCLK	1	Clock for SPI interface
MOSI	16	SPI-Master Out Slave In
MISO	15	SPI-Master In Slave Out
SSB	2	Slave Select – Active Low
DIAG	14	Diagnostic pad for measuring any of the internal voltages for debug purposes

4 Trigger Modes

There are 2 modes to trigger the measurement

Table 6 Trigger Modes

Radio Mode	Description
Pin based	The IC senses the relative difference between the inductance when EN to the IC is asserted
SPI based	The IC senses the relative difference between the inductance when a particular SPI command is given to the IC

5 Power Consumption in Different Modes

The following is the typical power consumption in the different radio modes

Table 7 Power Consumption in Different Modes

All typical values at +25 °C

IC Mode	Supply	Current Consumption (typ)	Unit
Idle	VLINE = 3.6 V	0.1	uA
Average current consumption in low sensitivity mode*	VLINE = 3.6 V	1.5	uA
Average current consumption in high sensitivity mode*	VLINE = 3.6 V	5	uA

Notes: *-Measured when the sensor triggered once in 70 ms

6 Interface with Microcontroller

Micro controller can interface with Au2001 using a simple SPI

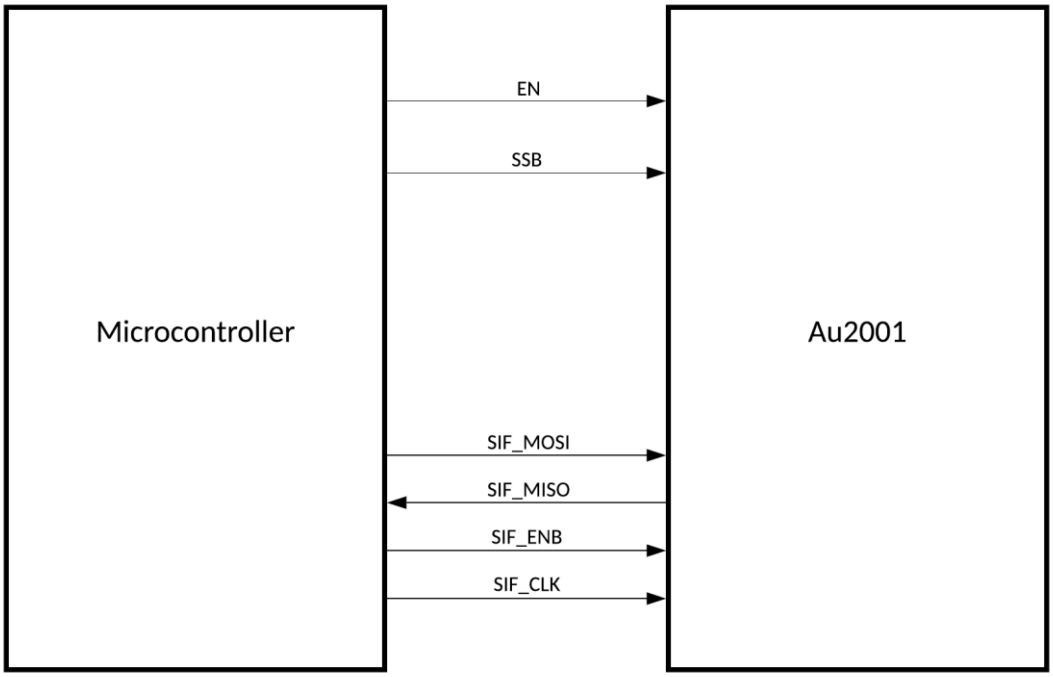

Figure 3 Microcontroller Interface

6.1 Timing sequence of a measurement cycle

6.1.1 Initial Sequence

When the sensor powers up for the first time, the microcontroller has to give a reset command to the sensor to reset the IC to a known initial state.

6.1.2 Measurement Sequence

There is a certain sequence of events that needs to be followed by the microcontroller to obtain the relative inductance change between the coils. The sequence of events are summarised below.

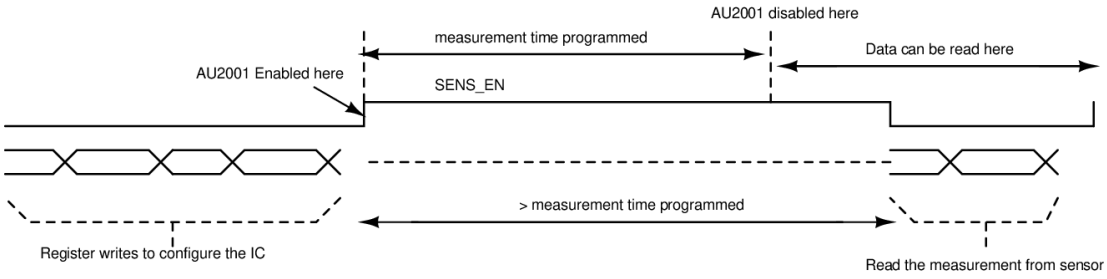

Figure 4 caption required

The above measurement sequence can be split-up into 3 sections

- **Configuration:** The microcontroller configures the Au2001 for various measurement parameters – Time for measurement (higher the time, higher the accuracy) and mode of measurement
- **Measurement:** To trigger the measurement, EN is asserted. EN has to be held high for a minimum duration of programmed measurement time mentioned in configuration and an additional time of 10 us. Once the measurement is done and the corresponding data is written to the registers, Au2001 is powered down automatically. Hence there is no limit on the maximum time for which EN has to be held high. EN signal should be deasserted and asserted again before the next measurement.
- **Data Read Back:** The data containing the information on relative inductance change can be read any time after the minimum duration. Data valid bit in the register indicates the validity of the data read. The data will be valid till the next measurement cycle triggered by assertion of EN signal.

6.2 One Time Calibration

Due to a variety of reasons, the 3 coils being fabricated in the PCB may not be matched to each other and there can be systematic mismatch between the inductance of these coils. One time calibration computes this mismatch and corrects for it. It is advisable to do the one time calibration on the final assembled water meter.

Sequence to be followed for one – time calibration is listed below

- Rotate the half-metal plate by blowing air or water through the pipe.
- While the half-metal plate is rotating, trigger measurements every fixed interval of 20 ms
- The calibration algorithm running in the MC will evaluate the average of data returned from coil1 (offset_coil1) and data returned from coil2 (offset_coil2)
- The offset values obtained from the above should be written in
    - SNS1_OFF0(0x06) and SNS1_OFF1 (0x07) for offset corresponding to coil1
    - SNS2_OFF0(0x08) and SNS2_OFF1 (0x09) for offset corresponding to coil2
- Stop the half metal plate rotation. Note that this offset should be written in non-volatile memory so that this is available for the microcontroller to read and write into the appropriate register everytime it powers up.

6.3 Run Time Calibration

If the Offset between the coils drift over time, run time calibration may be required. Based on the test results from set of boards, run time calibration may be implemented.

6.4 Serial Peripheral Interface

The Serial Peripheral Interface (SPI) in Au2001 is a slave only interface and supports both the conventional register access as well as short commands. To talk to the slave, the SPI master in the microcontroller has to be configured in the modes: clock polarity (CPOL) = 1 and clock phase (CPHA) = 1 or clock polarity (CPOL) = 0 and clock phase (CPHA) = 0. The data sent and received is aligned to the byte boundary.

6.4.1 Interface Signals

The Slave uses a four-wire serial interface. The signals in the interface are described below

Table 8 Interface Signals

Signal Name	Direction	Description
mosi	Input	SPI Master-Out-Slave-In (MOSI) signal
miso	Output	SPI Master-In-Slave-Out (MISO) signal
sclk	Input	SPI serial clock. The entire slave runs on this clock
csb	Input	SPI chip select. The signal has an active-low polarity

All control and data signals in the interface are assumed to be synchronous to the serial clock, sclk.

6.4.2 Serial Interface Timing at Bit-Level

A transaction is initiated by asserting the chip-select, csb (low), clocking the serial clock line (sclk) and driving the input data to the chip on mosi and sampling the output data from the chip on miso. The data is shifted in little-endian

format (MSB first), at bit level. The data sent or received must be aligned to the byte boundary. When csb is de-asserted, by default, the slave will leave the miso line floating. The bit-level timing can comply with two SPI modes, as shown in the figures below

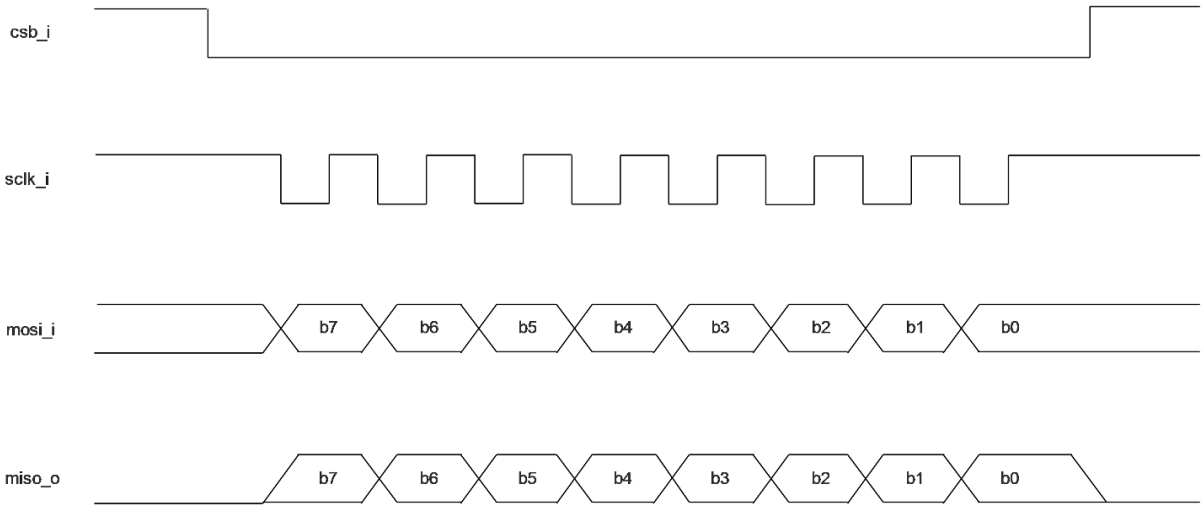

Figure 5 SPI timing for mode CPHA = 1 and CPOL = 1

In mode CPHA = 1 and CPOL = 1, the state of the clock line when csb is high is high. Both the master and slave drive data during the falling edge of sclk and sample data during the rising edge of sclk. Another SPI mode that is supported is mode CPHA = 0 and CPOL = 0. The bit-level timing for this mode is given below

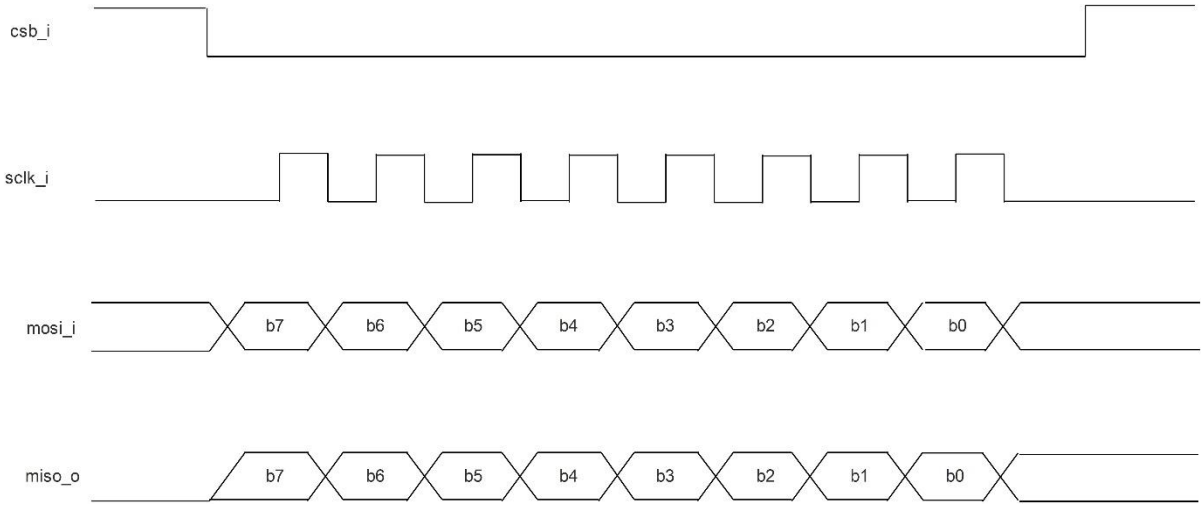

Figure 6 SPI timing for mode CPHA = 0 and CPOL = 0

In mode CPHA = 0 and CPOL = 0, the state of the clock line when csb is high is low. Both the master and slave drive data during the falling edge of sclk and sample data during the rising edge of sclk. As shown in the timing diagram, the MSB of the data has to be set-up before the first rising edge of sclk.

Since data is aligned to the byte boundary and given these timing specifications, the bit level timing information relative to sclk will be omitted from most of the subsequent figures, unless it is absolutely necessary.

6.4.3 Naming Conventions used while describing SPI

This section covers a few terms that used, while describing the SPI interface, in the rest of the document.

6.4.3.1 Transaction

An SPI transaction consists of a complete cycle where the csb is asserted, one or more bytes are sent and received and csb is de-asserted.

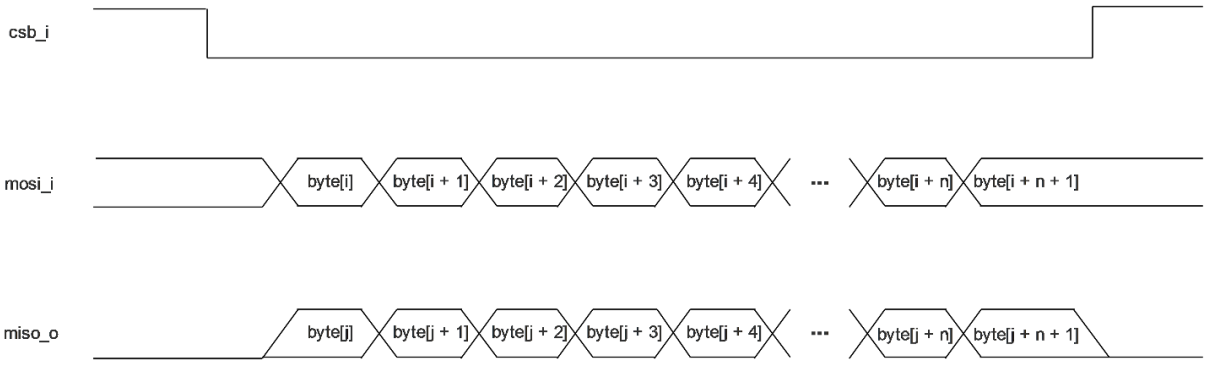

Figure 7 An SPI transaction, interpreted at byte level

6.4.3.2 Frame

One or more bytes sent during a transaction, may be a part of a larger word which is called a frame. The length of the frame in bytes is determined by a header, which is described in detail in the next section. A frame boundary is always referred with respect to the data sent by the master. A frame cannot spread across two transactions.

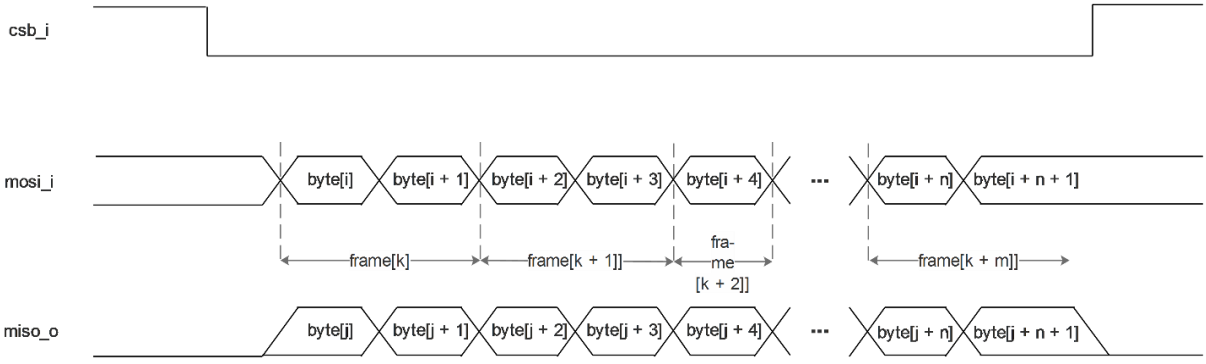

Figure 8 An SPI transaction, interpreted at frame level

6.4.3.3 Command and Arguments

Every frame sent by the master begins with a two-bit header called a command. The command decides the frame length and frame format. Additional bits in the frame may constitute arguments to the command, as prescribed by the frame format. The last argument may be padded with zeros on the LSB side, to align the frame to the byte boundary.

Table 9 Generic Frame Format

Command (2 bits)	Argument 1	Argument 2	. . .	Argument n	Zero-padding (optional)

6.4.3.4 Data from slave and address pointer

While the master can send frames of different lengths to the slave, which specify different commands, the data sent by the slave is always the data at a particular address in the register map in the slave. The slave has 64 configuration and control registers, each one byte long. Every byte sent by the slave is the data at one of these registers. An internal address pointer decides the register whose data will be sent by the slave, when the next byte is being transferred over SPI from the slave to the master. The address pointer gets updated during or after a frame in sent by the master.

6.4.3.5 SPI Commands

This section describes various commands supported by the slave and the associated frame formats. The commands are summarized in the table below and described in detail in the subsequent sections.

Table 10 SPI Commands

Command	Header code	Description
Reset	0x03	Resets all configuration and control registers to their defaults.
Execute sub-command	0x02	Executes a sub-command, specified by the argument.
Write register	0x01	Writes to a register in the register map
NOP/Read register	0x00	No action taken/Reads from a register in the register map

Many commands accept a register address as their argument. This address is copied to the internal address pointer in the slave. The first byte sent by the slave during the next frame is the data at this address. If the frame is longer than one byte, the data sent by the slave during other bytes in the frame is specified in the frame format.

6.4.3.6 Reset

This command resets the configuration registers in the register map and all other control registers in the chip. The reset command frame is one byte long. This command accepts the address of the register to be read during the next transaction as an argument.

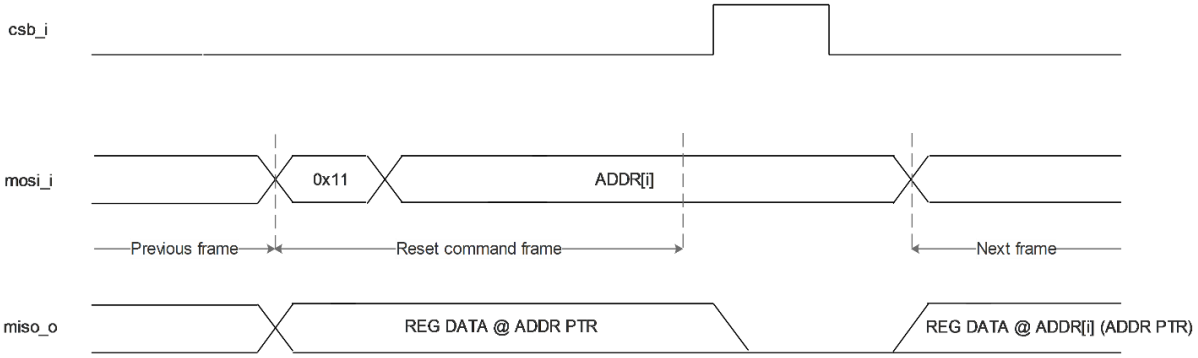

Figure 9 Reset Command Frame

6.4.3.7 Execute sub-command

This command frame in one byte long and executes a sub-command. The sub-command to be executed is specified as an argument, by a 3-bit code. Zeros are padded to align the frame to the byte boundary. The frame format is given below

Table 11 Execute Sub-Command Command Frame Format

7 : 6	5 : 3	2 : 0
0x02	Sub-command code	0x00

Various sub-commands are given in the table below

Table 12 Sub-Command Description

Sub-command code	Sub-command	Description
0x00	Go	sub_cmd_go_o is asserted, after the sub-command code is shifted in and before the end of the frame. The signal stays high for at least 3 SPI clock cycles and is de-asserted either before the end of the next frame or when csb_i is deasserted, whichever event occurs earlier
Others	-	Unimplemented. The slave is expected to ignore these codes

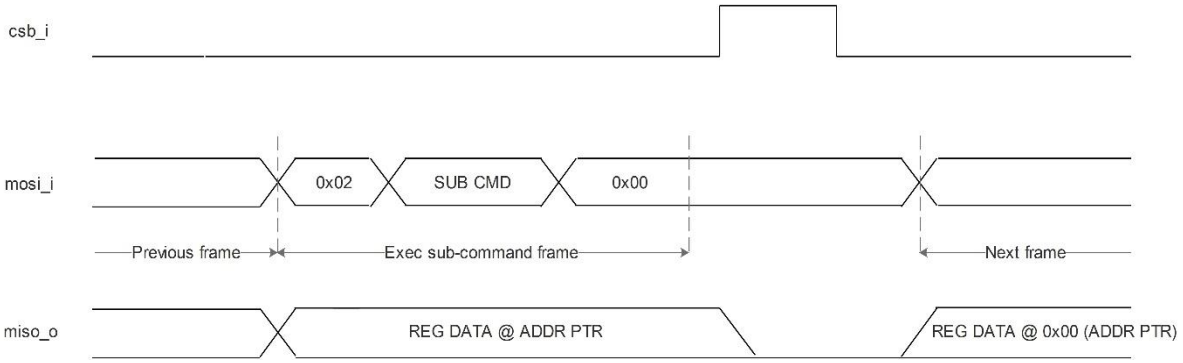

Figure 10 Execute Sub-Command Command Frame Format

During this frame, the internal address pointer is set to zero. So, first byte sent by the slave during the next frame will be the data at register address 0x00.

6.4.3.8 Write Register

The write register command frame is two bytes long and performs write to a configuration register in the slave. The command accepts the address of the register to be written and the data to be written to the register as arguments.

Table 13 Write Command Frame Format

15 : 14	13 : 8	7 : 0
0x01	Address of register to be written	Data to be written to the register

The timing diagram for this frame is given below

During the first byte of this frame, the slave sends the data at the register address stored in the internal address pointer. At the same time, the address of the register to be written, as specified by the master, is copied to the address pointer. During the second byte of this frame, the slave sends the data at the address to be written, specified by the master (old data). At the same time, the data to be written, as specified by the master, is copied to the register. During the next frame, the first byte sent by the slave is the new data at this address.

6.4.3.9 No operation (NOP)/Read register

The NOP command frame is one byte long and causes the slave to take no action. The command accepts the register to be read during the next frame as an argument. The address is copied to the internal address pointer. The frame format is given below

Table 14 NOP/Read Command Format

7 : 6	5 : 0
0x00	Register to be read during the next frame

The timing diagram for this frame is given below

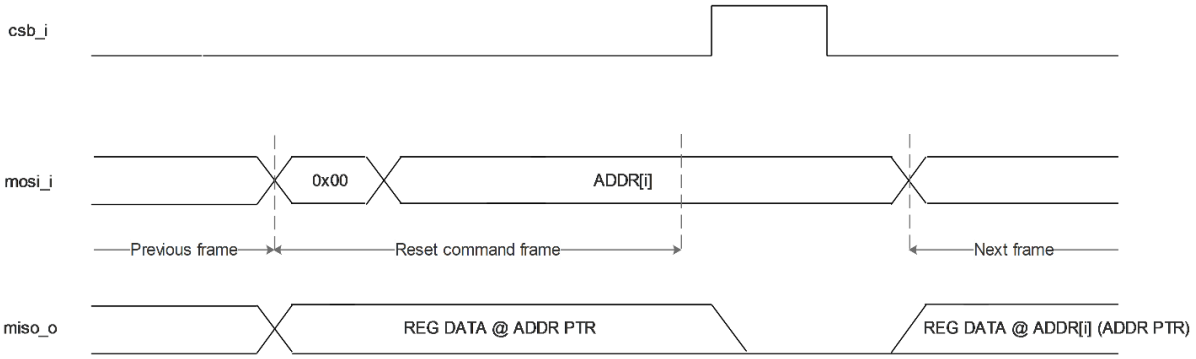

Figure 11 NOP/Read Command Format

7 Application Diagrams

7.1 Interface with Microcontroller and Inductance

The figure below shows the normal use case where Au2001 is used as a sensor interfacing with 3 PCB inductance and microcontroller

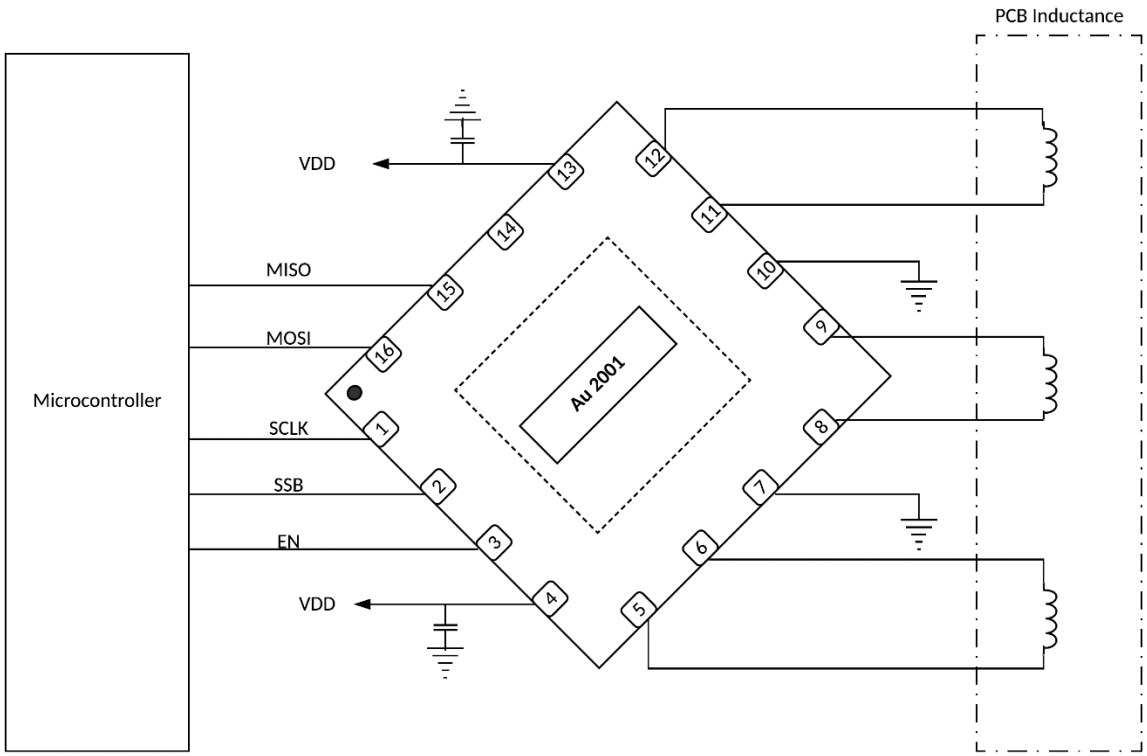

Figure 12 Application Schematic

8 PCB Inductance Layout Guidelines

The following layout guidelines should be followed for getting performance

- The WM IC should be placed in the centre of the inductance. The IC and the inductance should be placed in the same plane.
- The outer loop of the inductance should be dictated by the size of the metal plate
- All 3 inductance should form an angle of 120 to each other w.r.t the centre of the IC

9 Trademarks

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10 Contact Information

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